What is claimed is:

1. A method of manufacturing a thin film transistor comprising:

forming a semiconductor region having an island shape on an insulating substrate;

forming a gate electrode above the semiconductor region with a gate dielectric film being provided therebetween;

Implanting an impurity to the semiconductor region using the gate electrode as a mask, in order to form source and drain regions in a self-aligned manner at both sides of a channel region;

forming an interlayer dielectric film on the gate electrode and the gate dielectric film; and

simultaneously activating the impurity and burning the interlayer dielectric film through a single heat treatment.

2. The method of manufacturing a thin film transistor according to claim 1, wherein the semiconductor region having an island shape is formed on an undercoat layer formed on the insulating substrate.

3. The method of manufacturing a thin film transistor according to claim 2, wherein the undercoat layer has a two-layer structure including a silicon nitride layer and a silicon oxide layer.

4 The method of manufacturing a thin film transistor according to claim 1, wherein the semiconductor region having an island shape is formed by:

forming an amorphous silicon layer;

causing the amorphous silicon layer to become a polycrystalline silicon layer by the use of an excimer layer; and

patterning the polycrystalline silicon layer.

5. The method of manufacturing a thin film transistor according to claim 4, wherein the amorphous silicon layer is

caused to become the polycrystalline silicon layer after the amorphous silicon layer is annealed to evaporate hydrogen, thereby lowering a hydrogen concentration.

6. The method of manufacturing a thin film transistor according to claim 4, wherein after implanting the impurity to form the source and drain regions, a hydrogen plasma treatment by a plasma CVD method is performed to terminate dangling bonds of the polycrystalline silicon layer with hydrogen.

7. The method of manufacturing a thin film transistor according to claim 1, wherein the interlayer dielectric film is formed of an organic insulating material or an inorganic insulating material containing silicon atoms and oxygen atoms as major components.

8. The method of manufacturing a thin film transistor according to claim 7, wherein the burning is performed for an hour at a temperature selected from the group consisting of 350°C, 400°C, 450°C, and 500°C.

9. The method of manufacturing a thin film transistor according to claim 6, wherein a second silicon nitride layer for preventing hydrogen terminating the dangling bonds from desorbing from the dangling bonds is formed as an underlying layer of the interlayer dielectric film.

10. The method of manufacturing a thin film transistor according to claim 9, wherein the second silicon nitride layer has a thickness of 200 nm.

11. The method of manufacturing a thin film transistor according to claim 10, wherein the heat treatment is performed at 400°C for an hour.

12. A method of manufacturing a flat panel display including

pixels arranged in a matrix form, and displaying an image by individually turning on or off a transistor of each pixel, the method including a method of manufacturing the transistor, comprising:

forming a semiconductor region having an island shape on an insulating substrate;

forming a gate electrode above the semiconductor region with a gate dielectric film being provided therebetween;

implanting an impurity to the semiconductor region using the gate electrode as a mask, in order to form source and drain regions in a self-aligned manner at both sides of a channel region;

forming an interlayer dielectric film on the gate electrode and the gate dielectric film; and

simultaneously activating the impurity and burning the interlayer dielectric film through a single heat treatment.

13. The method of manufacturing a thin film transistor according to claim 12, wherein the semiconductor region having an island shape is formed on an undercoat layer formed on the insulating substrate.

14. The method of manufacturing a thin film transistor according to claim 12, wherein the undercoat layer has a two-layer structure including a silicon nitride layer and a silicon oxide layer.

15 The method of manufacturing a thin film transistor according to claim 12, wherein the semiconductor region having an island shape is formed by:

forming an amorphous silicon layer;

causing the amorphous silicon layer to become a polycrystalline silicon layer by the use of an excimer layer; and

patterning the polycrystalline silicon layer.

16. The method of manufacturing a thin film transistor

according to claim 15, wherein the amorphous silicon layer is caused to become the polycrystalline silicon layer after the amorphous silicon layer is annealed to evaporate hydrogen, thereby lowering a hydrogen concentration.

17. The method of manufacturing a thin film transistor according to claim 15, wherein after implanting the impurity to form the source and drain regions, a hydrogen plasma treatment by a plasma CVD method is performed to terminate dangling bonds of the polycrystalline silicon layer with hydrogen.

18. The method of manufacturing a thin film transistor according to claim 12, wherein the interlayer dielectric film is formed of an organic insulating material or an inorganic insulating material containing silicon atoms and oxygen atoms as major components.

19. The method of manufacturing a thin film transistor according to claim 18, wherein the burning is performed for an hour at a temperature selected from the group consisting of 350°C, 400°C, 450°C, and 500°C.

20. The method of manufacturing a thin film transistor according to claim 17, wherein a second silicon nitride layer for preventing hydrogen terminating the dangling bonds from desorbing from the dangling bonds is formed as an underlying layer of the interlayer dielectric film.

21. The method of manufacturing a thin film transistor according to claim 20, wherein the second silicon nitride layer has a thickness of 200 nm.

22. The method of manufacturing a thin film transistor according to claim 21, wherein the heat treatment is performed at 400°C for an hour.

23. A thin film transistor comprising:

an insulating substrate;

a channel region serving as a central portion of a semiconductor layer having an island shape formed on the insulating substrate;

a pair of source and drain regions formed at both sides of the channel region in the semiconductor layer;

a desorption preventing layer formed to cover at least the channel region and the source and drain regions for preventing hydrogen terminating dangling bonds of the semiconductor layer from desorbing from the dangling bonds; and

an interlayer dielectric film formed on the desorption preventing layer.

24. A flat panel display including pixels arranged in a matrix form, and displaying an image by individually turning on or off a transistor of each pixel, the transistor comprising:

an insulating substrate;

a channel region serving as a central portion of a semiconductor layer having an island shape formed on the insulating substrate;

a pair of source and drain regions formed at both sides of the channel region in the semiconductor layer;

a desorption preventing layer formed to cover at least the channel region and the source and drain regions for preventing hydrogen terminating dangling bonds of the semiconductor layer from desorbing from the dangling bonds; and

an interlayer dielectric film formed on the desorption preventing layer.